# (12)UK Patent Application (19)GB (11) 2 059 724 A

(54) **Data transmission systems**

(57) A data transmission system comprises a transmitter 5 transmitting data messages to receivers 8, 10, 12 ... n by means of a link 6. Each message is preceded by a preamble, which is such that it can either be recognised only by one of the receivers (to which, alone, the message is directed) or it can be recognised by all receivers when the message is intended for all of them. Each preamble is recognised if at least x of its y bits are recognised. At each receiver, the received preamble is sampled at a multiple of the bit rate and the respective pulse trains produced by the same-numbered samples in each bit period are individually compared with the two predetermined preambles to be recognised by that receiver. The identities of the pulse trains which match either of the predetermined preambles are recorded and the clock in the receiver is then phase-shifted so as to centre its bit periods with the sampling pulses producing that one of the matching pulse trains whose sampling pulses are time-positioned midway of the sampling pulses producing all the matching pulse trains. The sampling rate is then reduced to bit rate, and the receiver is thus synchronised with the bit rate of the incoming message.
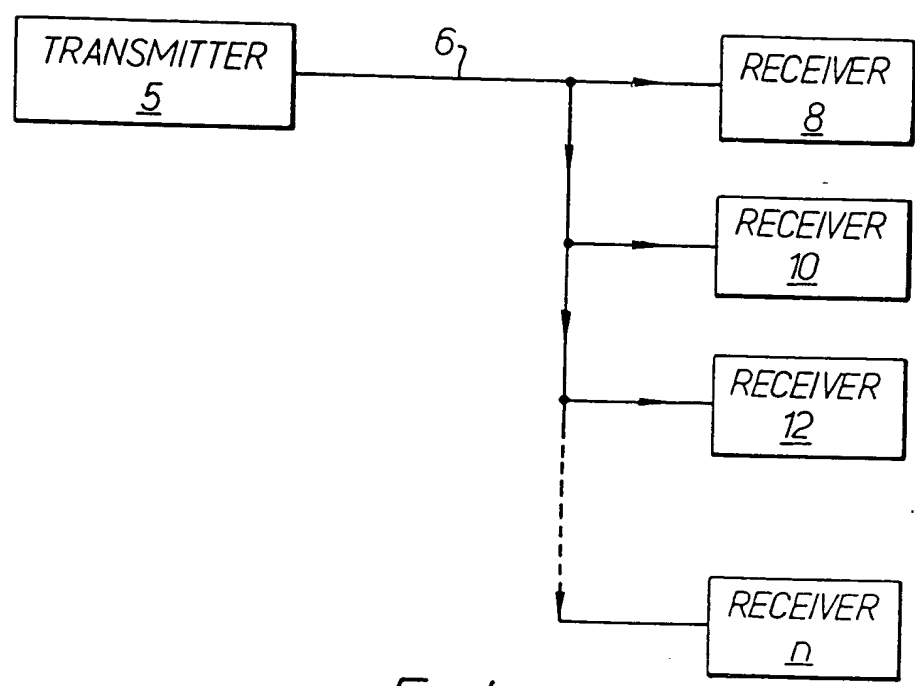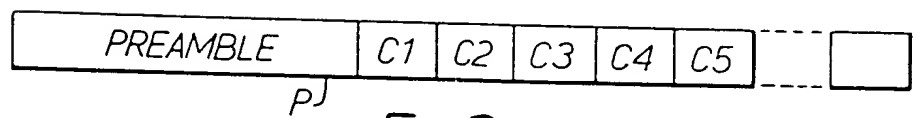
FIG.1.

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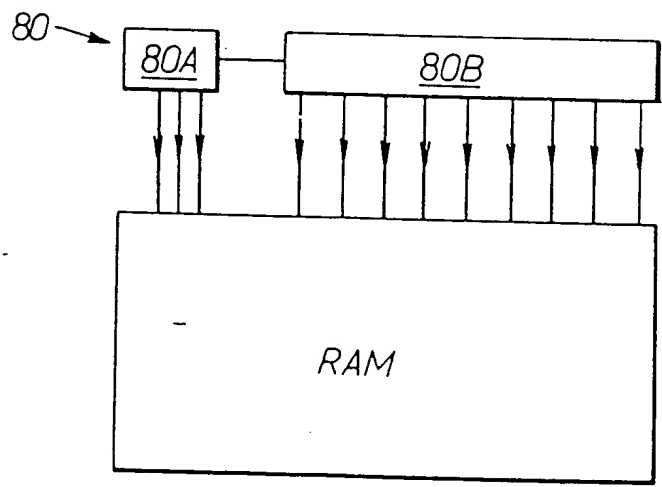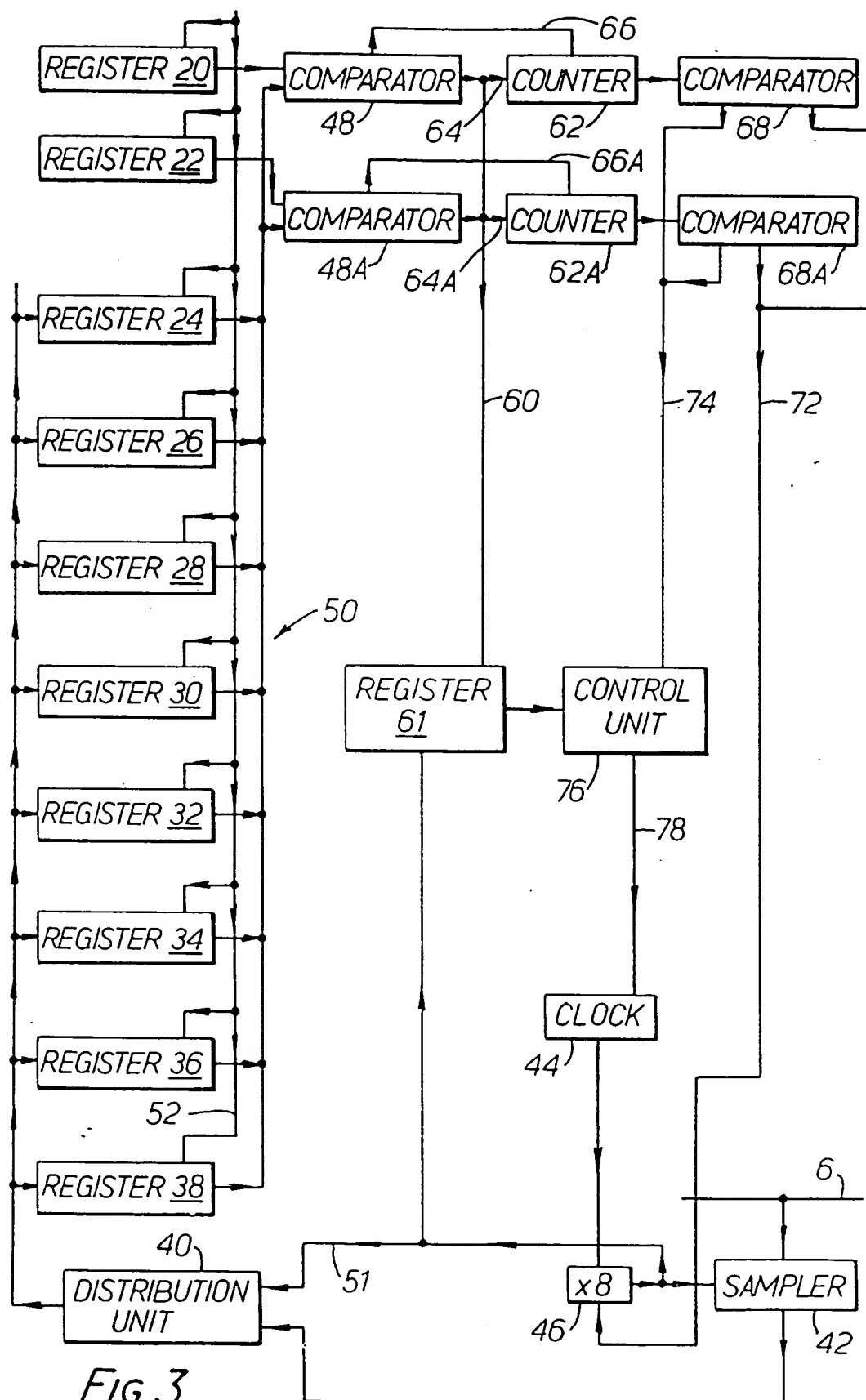
2059721



FIG.1.



FIG.2.



FIG.5.

2050724
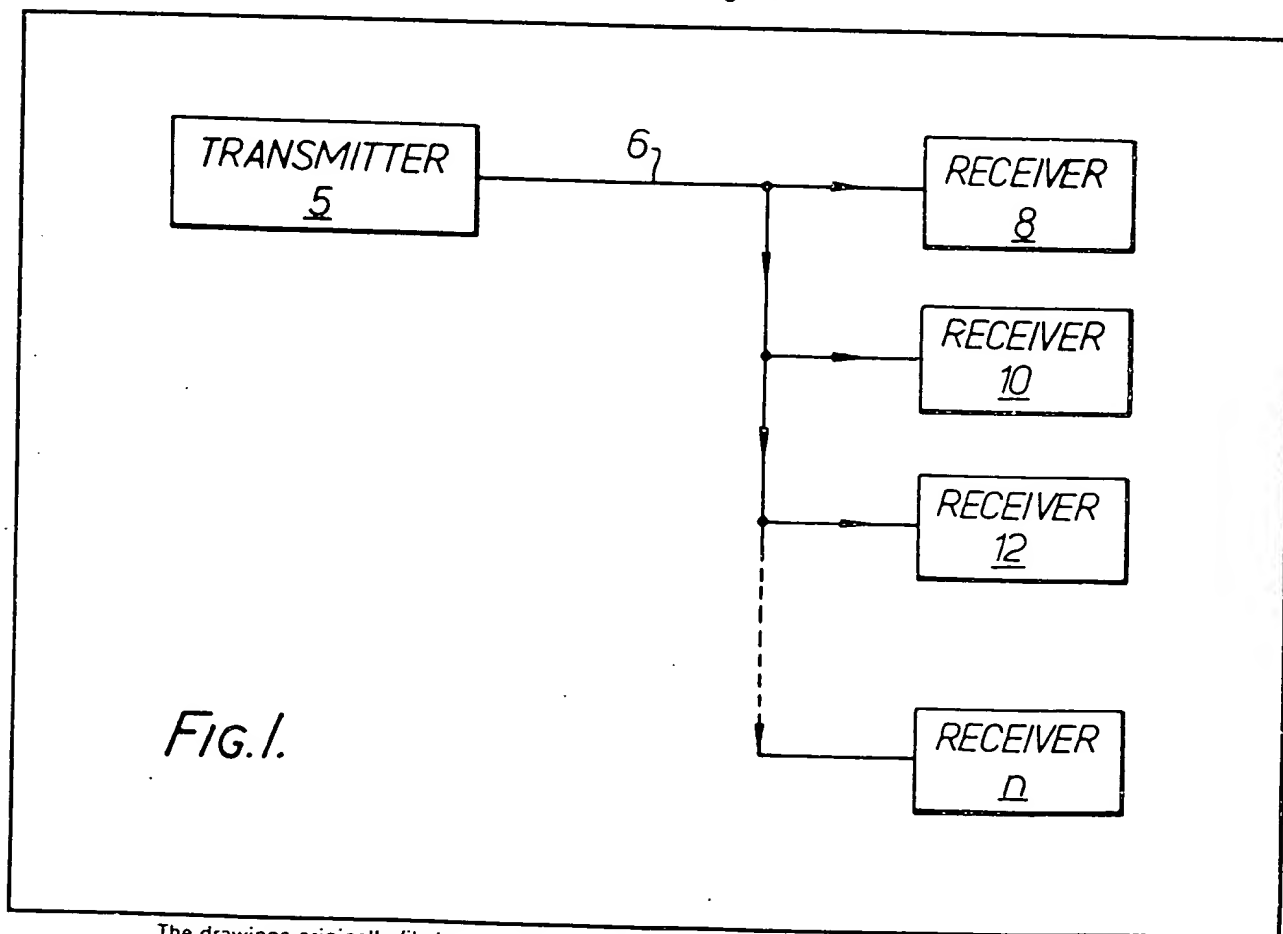


FIG.3.

FIG.4.
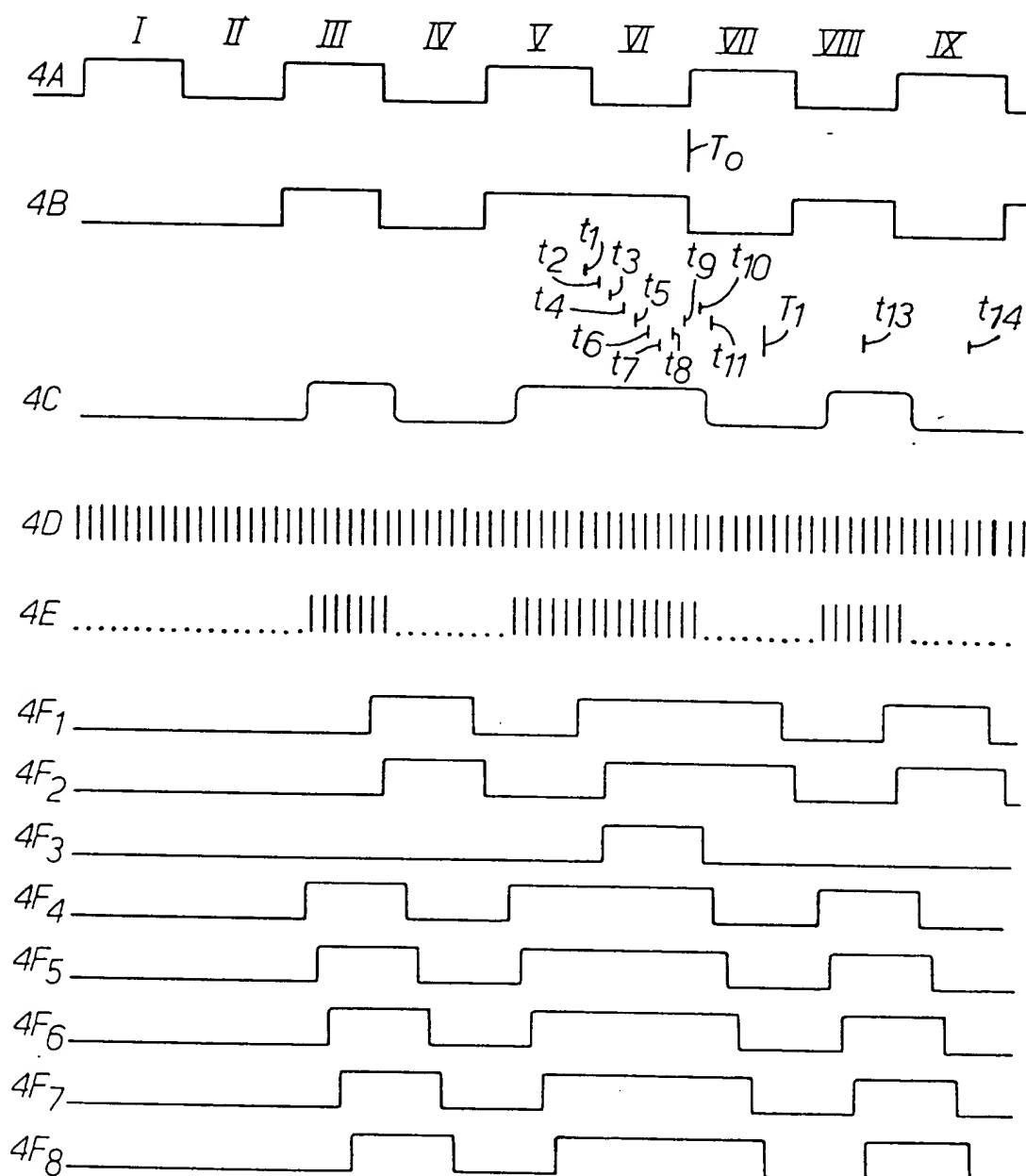
SPECIFICATION

**Improvements in and relating to data transmission systems**

5  The invention relates to data transmission systems.                                                             5
     Various novel features of the invention will be apparent from the following description, given
by way of example only, of data transmission systems embodying the invention, reference being
made to the accompanying diagrammatic drawings in which:
     *Figure 1* is a block diagram of one of the systems;
10   *Figure 2* is a diagram showing the form in which data characters are transmitted in the system   10
of Fig. 1;
     *Figure 3* is a more detailed block diagram of one of the receivers in the system;
     *Figure 4* shows waveforms occurring in the system; and
     *Figure 5* shows part of the block diagram of Fig. 3 in more detail.
15   As will be more specifically described, a data transmission system for transmitting data          15
messages from a data transmitter to a specific one of a plurality of receivers to which the
transmitter is connected by a transmission link comprises preamble generating means in the
transmitter for immediately preceding each data message with a predetermined preamble which
is intended to be recognisable by one of the receivers, to which the message is directed, but not
20  by others of the receivers to which the message is not directed, recognition means in each of     20
the receivers for testing for recognition each preamble received via the transmission link, and
synchronisation means in each receiver which is responsive to each recognised preamble for
synchronising that receiver with the data message immediately following the preamble.
     The recognition means may be arranged to recognise a preamble if it recognises at least a
25  predetermined part thereof, the said part being such in relation to expected errors in the         25
transmission link, that the probability is high that the recognition means will recognise the
correct preamble and being such that the probability is low that the recognition means will
recognise noise as the correct preamble.
     Advantageously, the preamble generating means generates each preamble as a plurality of
30  data bits, and each recognition means comprises means in each receiver for comparing each         30
preamble received on the transmission link with a predetermined preamble stored in that
receiver, and means for indicating recognition when at least a predetermined plurality of bits
forming the said predetermined part of the received preamble agree as to value and position
with corresponding bits forming part of the stored preamble.
35   The preamble generating means in the transmitter may include means for generating a             35
preamble which is intended to be recognisable by a plurality of the receivers.
     Also to be described is a data transmission system, comprising a data transmitter connected
by a transmission link to a plurality of data receivers for sending data messages to any specific
one of the receivers, comprising preamble generating means at the transmitter for preceding
40  each data message with a selected one of a plurality of different predetermined preambles and    40
for transmitting the selected preamble to all the receivers immediately before the data message,
one of the preambles being recognisable by all the receivers and each of the remaining
prambles being recognisable only by a specific one of the receivers, and recognition means in
each receiver for recognising either the said one preamble or the respective one of the remaining
45  prembles and, in response to such recognition, for receiving the immediately following data      45
message. In such a case, the preamble generating means preferably generates each preamble
such that the Hamming distance between any pair of them is large. For example, each preamble
may comprise a predetermined plurality of serial digits, and in which case the preamble
generating means may comprise means responsive to two basic sequences of serially arranged
50  digits for carrying out a succession of adding operations each comprising the addition of each of  50
the digits of one of the basic sequences to a respective one of the digits of the other basic
sequence, whereby each adding operation produces a respective one of the said preambles, the
first adding operation comprising the addition of each digit in one basic sequence to the same
serially numbered digit in the other basic sequence, the next adding operation involving the
55  addition of each digit in one of the basic sequences to the digit in the other basic sequence     55
having a serial number greater by one (with the last digit of the first sequence being added to
the first digit of the second sequence), the third adding operation involving the addition of each
digit in the first sequence to the digit of the second sequence having a serial number greater by
2 (with the penultimate and last digits of the first sequence being added to the first and second
60  digits, respectively, of the second sequence), and so on for the remaining adding operations.     60
     Advantageously, the recognition means in each receiver comprises means operative to
compare the digits of an incoming transmitted preamble with the digits of the predetermined
preamble of that receiver, and means for indicating recognition when at least a predetermined
block of incoming digits agrees digit by digit with a corresponding block of the digits of the
65  predetermined preamble, the predetermined block being such in relation to digits of the whole     65

predetermined preamble and to the expected occurrence of transmission errors on the transmission link that the probability of any of the recognition means recognising the correct preamble is high and the probability of its recognising noise on the transmission link as the correct preamble is low.

5    Further to be described is a data transmission system, comprising a data transmission connected to a data receiver by a data transmission link, means in the transmitter for transmitting to the receiver a predetermined waveform having a predetermined frequency, means in the receiver and operative at a predetermined multiple of a reference frequency which is equal to the predetermined frequency but not necessarily in phase therewith to produce

10   successive amplitude samples of each cycle of the predetermined waveform, means responsive to the samples to produce a plurality of pulse trains the first of which comprises pulses respectively dependent on the first amplitude sample in each period of the predetermined waveform, the second of which comprises pulses respectively dependent on the second amplitude sample of each cycle of the predetermined waveforms, and so on for the remaining

15   pulse trains, means operative to compare each pulse train with a waveform corresponding to the predetermined waveform to determine which of the pulse trains have waveforms corresponding with the predetermined waveform and which do not, means operative in response to the pulse trains detected as having waveforms agreeing with the predetermined waveform to assess the serial position within a period of the reference frequency of the samples producing those pulse

20   trains to identify the central one of those serial positions, and phase-shift means operative to phase-shift the reference frequency of the receiver to bring it into phase with the central one of those serial positions, whereby to synchronise the reference frequency of the receiver with the predetermined frequency.

Such a system preferably includes means for counting the number of pulse trains which are

25   detected as having waveforms agreeing with the predetermined waveform and for preventing operation of the phase-shift means until the number counted is at least equal to a predetermined number which is less than the number of the samples within each period of the reference frequency.

As shown in Fig. 1, the system comprises a data transmitter 5 from which the data originates

30   and which is connected by a suitable data transmission link 6 to data receivers 8, 10, 12 ... n.
The system is arranged to transmit data in a manner which enables the data to be addressed either to any specific one of the receivers (so as to be recognised and received by that receiver but not by the other receivers) or to all the receivers (this is termed the "broadcast" mode).
Fig. 2 shows diagrammatically the manner in which data is transmitted.

35   As shown, the data is transmitted in the form of characters C1, C2, C3 ... each of which contains the same predetermined number of, in this example, binary digits. Each message (that is, a number of successive characters) is preceded by a preamble P. The preamble is also made up of a predetermined number of bits.
In a manner to be described, the system is arranged so that each receiver is able to use the

40   preamble for three functions:—
(a) for character framing, that is, to recognise that a data message is about to begin and begins immediately after the end of the preamble;
(b) as an address, that is, to determine whether or not the data message which is about to begin is intended for that receiver specifically or wheher it is a message being transmitted

45   in the broadcast mode;
(c) for bit synchronisation, that is, to enable the receiver to synchronise itself with the bits of the data message.
The end of the message is signified by a postamble which will not be discussed further.
In order to achieve the second of the three functions, that is, the addressing function, the

50   system is arranged to be able to produce (n + 1) different preambles. Of these, each of n of them is recognised by a respective one of the receivers as indicating that the message following is intended for that receiver alone, while the (n + 1)th preamble is recognised by all the receivers as indicating that the message following is transmitted in the broadcast mode and is therefore to be received by all the receivers. Therefore, each message transmitted by the transmitter 5 is

55   preceded by the appropriate one of the preambles in order to achieve the addressing function and each receiver must be capable of recognising two preambles.
Each preamble contains y bits. In a manner to be explained in more detail the system is arranged so that each receiver can recognise either of its two preambles provided that it is able to recognise at least x bits of the preamble, where x is less than y. Therefore, up to (y − x) errors

60   can be incurred in a preamble and the receiver or receivers for which it is intended will still recognise it. Each receiver holds in store the two preambles which it is to be capable of recognising. Each receiver inspects each incoming bit and makes two comparisons: each is a comparison between, on the one hand, a block of data comprising that bit and the previous (y − 1) bits and, on the other hand, the y bits of a respective one of the two predetermined

65   preambles which it is storing. If at least x bits of the two blocks compared in either of the two

comparisons agree, then the receiver recognises the preamble and accepts the next bit as the first bit of the first character of a message intended for that receiver.

x is chosen so that the probability of accepting the preamble (assuming that it is sent) is high (e.g. 0.95) in relation to the mean error rate expected for the transmission link, and so that the
5 probability of the receiver accepting a preamble when in fact no preamble was sent, and there is just noise on the line, is very low (typically $10^{-8}$). x must not be so high in relation to the expected error rate for the transmission link that transmission errors are likely to cause the receiver to fail to recognise a preamble as one of its stored preambles. In addition, each preamble needs to be designed so that the receiver has a low probability of recognising a
10 correctly transmitted and received preamble until it has compared all y bits of that preamble with the stored bits of its two specific preambles (and found that at least x bits of the received preamble agree with x bits of one of its two stored preambles). If the preambles were designed such that a receiver could (assuming no transmission errors) recognise a preamble as being one of its stored preambles before all the y bits of the incoming preamble had been received, then it
15 would incorrectly assume that the (x + 1)th bit of the received preamble was the first bit of the first character of the message.

Preferably, the system uses preambles which each have a two-valued autocorrelation function.

In order to ensure that there is a very small probability of a receiver incorrectly recognising the preamble of a message intended for one of the other receivers, the (n + 1) preambles are
20 designed such that every pair of them have a large difference, that is, have a large Hamming distance between them. Advantageously, they are designed such that the Hamming distance between every pair of them is greater than 2(y − x).

In a manner to be more specifically described, this may be achieved by producing the preambles from two basic bit sequences, I and II, where
25    $I = a_1, a_2, a_3, \ldots a_y$; and
$II = b_1, b_2, b_3, \ldots b_y$.
Then, in order to produce the first of the (n + 1) preambles, I and II are added together to produce a first preamble, $P_1$, where
$P_1 = (a_1 + b_1), (a_2 + b_2), (a_3 + b_3), \ldots (a_y + b_y)$.
30 The second preamble, $P_2$, is produced by phase-shifting one of the basic bit sequences I and II by one bit and then adding it to the other basic bit sequence, so as to produce
$P_2 = (a_1 + b_2), (a_2 + b_3), (a_3 + b_4) \ldots (a_y + b_1)$.
This process is repeated so as to produce further preambles, e.g. $P_3$ and $P_4$:
$P_3 = (a_1 + b_3), (a_2 + b_4), (a_3 + b_5) \ldots (a_y + b_2)$;
35    $P_4 = (a_1 + b_4), (a_2 + b_5), (a_3 + b_6) \ldots (a_y + b_3)$.
This process is repeated to produce the requisite number of preambles (assuming that (n + 1) is less than y).

The method by which each receiver is brought into bit-synchronisation with a message addressed to it will now be described with reference to Fig. 3 showing one of the receivers in
40 block diagram form.

As shown, the receiver comprises two registers 20 and 22 which respectively store the two preambles (referred to below as $P_a$ and $P_b$) to be recognised by that receiver. In addition, the receiver includes eight further registers 24 to 38 each having a capacity of y bits.

The registers 24 to 38 are connected to receive samples of the incoming data in a manner to
45 be explained, this incoming data being distributed to the eight registers by a distribution unit 40. The data samples are produced by sampling gate 42 connected to the transmission link 6. The sampling gate 42 is controlled by clock signals produced by the receiver's clock pulse source 44 which are fed to the sampling gate 42 via a multiplier 46 having (in this example) a multiplication factor of 8.
50 The bits in each of the registers 24 to 38 can be compared, bit by bit, with the bits in each of the registers 20 and 22 by means of respective comparators 48 and 48A. The bits are fed from each of the registers 24 to 38 to the comparators 48 and 48A by means of a data channel 50.

The operation of the receiver as so far described will now be explained with reference to Fig. 4.
55    Fig. 4A shows nine clock periods numbered I to IX of the receiver clock 44.

It will be assumed that the transmitter is transmitting on the link 6 the preamble of a message intended for the particular receiver under consideration. The waveform of the preamble as received by the receiver is shown in bit periods I to VI of Fig. 4C (the data message starts at time $T_o$). It will also be assumed that the preamble is being received without error. However, as
60 is shown by a comparison of waveform 4C with waveform 4A, the preamble is not being received in bit-synchronisation with the receiver clock. Furthermore, it has been distorted by transmission, from a pure rectangular waveform. Waveform 4B shows the waveform which the preamble would have if it were being received in bit-synchronisation with the receiver clock and with no distortion. Waveform 4B therefore represents the waveform produced if the preamble $P_a$
65 stored in register 20 were to be read out in bit-synchronisation with the receiver clock 44. In

this example, the preamble consists of six bits 0 0 1 0 1 1 (in Fig. 4, a high level represents a "1", a low level represents a "0").

Before the receiver can begin to receive the data message, its clock pulse waveform must be bit-synchronised with the message—so that the receiver can correctly sample the first bit of the
5 message at its mid point ($T_1$). 5

In order to carry out this synchronising process, the sampling gate 42 (Fig. 3) is operated at a multiple of the clock frequency—because the clock signals from the clock 44 are fed to the sampling gate 42 via the multiplier 46 which, in this example, has a multiplication of 8. The sampling instants are therefore as shown in waveform 4D. Waveform 4E shows the samples
10 taken of waveform 4C at the sampling instants of waveform 4D. A dot signifies a "0", a vertical 10 line signifies a "1".

The data samples taken by the sampling gate 42 are directed into the eight registers 24 to 38 in sequence by the distributing unit 40. This is controlled, via line 51, in synchronism with the sampling pulses produced by the multiplier 46 so that the data samples taken at the first
15 sampling instant in each cycle of the clock waveform are all fed into register 24, the data 15 samples taken at each second sampling instant are fed into register 26, and so on for the remaining data samples, so that the data samples taken at each eighth sampling instant are fed into register 38. Each register 24 to 38 can hold six bits.

After each data sample has been fed into its appropriate register 24 to 38, the contents of
20 that register are rapidly fed out onto the channel 50 by means of timing signals occurring on a 20 line 52 at a multiple of the sampling rate. Synchronously with this, the bits of the stored preambles $P_a$ and $P_b$ are fed out of the registers 20 and 22. Therefore, each comparator 48, 48A makes a bit by bit comparison of the y bits (where y = 6 in the present example) of the corresponding one of the stored preambles $P_a$ and $P_b$ with the y data samples from the particular
25 one of the registers 24 to 38 being interrogated. Thus, more specifically, during each bit period 25 of the receiver clock, the comparator 48 carries out eight comparisons in sequence:— first, it compares the value of the data sample taken at the first sampling instant of that bit period, together with the values of the data samples taken at the first sampling instants during the previous (y − 1) or five (in this example) bit periods, with the six bits of the stored preamble $P_a$
30 in register 20; secondly, it compares the value of the data sample taken at the second sampling 30 instant in that bit period, together with the values of the data samples taken at the second sampling instants in the previous five bit periods, with the preamble $P_a$ stored in register 20; and so on for the remaining six sampling instants of that bit period. Comparator 48A carries out eight similar comparisons at the same time, but of course these are made with the preamble $P_b$
35 stored in register 22. 35

Waveform $4F_1$ shows how the data samples stored in register 24 (the data samples taken during the first sampling instants) can be represented, while waveforms $4F_2$ to $4F_8$ show how the data samples in registers 26 to 38, respectively, can be represented. In effect, therefore, comparator 48 makes a bit by bit comparison of each of the waveforms $4F_1$ to $4F_8$ in turn with
40 the waveform 4B (in waveforms $4F_1$ to $4F_8$, the sample pulses stored in the registers 24 to 38 40 are each shown stretched out to the length of a bit period to enable the waveforms to be more easily compared with the waveform 4B). Comparator 48A operates in similar fashion but of course it compares each of the waveforms $4F_1$ to $4F_8$ in turn with the waveform (not shown) of the preamble assumed to be stored in register 22.
45 Each comparator is arranged to produce a "1" when it makes a successful comparison, that 45 is, when it determines that at least x bits of the two waveforms being compared agree (where x is as discussed above). If the comparison is unsuccessful (less than x bits agree), the comparator produces a "0" output. When the comparator 48 makes the first successful comparison after an unsuccessful comparison it energises a line 60 which causes the identity of the particular one of
50 the registers 24 to 38 producing the successful comparison to be stored in a memory 61. In 50 other words, memory 61 identifies which of the eight sampling instants in a bit period produced this first successful comparison.

As shown in Fig. 3, each "1" output of comparator 48 is fed to a counter 62 on a line 64 and increments the count of the counter 62 by 1. When the comparator 48 produces a "0"
55 output this is fed to the RESET input of the counter 62 by means of a line 66 and resets the 55 counter to zero. Each "0" output from comparator 48 also causes the immediately previous count in the counter 62 to be fed into a further comparator 68 where the value of the count is compared with a threshold number which is less than the number of data samples being taken during each bit period of the receiver. Therefore, in the example being considered, this threshold
60 number is less than eight and may be, say, six. In response to each unsuccesful comparison by 60 the comparator 48, the comparator 68 therefore determines how many successful comparisons occurred immediately preceding the unsuccessful comparison. If comparator 68 determines that the number of successful comparisons recorded by the counter 62 is less than the threshold number (6 in this example), the process repeats and the counter starts again to count the
65 successful comparisons as they occur. However, if the comparator 68 determines that the 65

number of successful comparisons recorded by the counter 62 at that time is more than the threshold number, it switches off the multiplier 46 by means of a line 72 so that the sampling gate 42 now samples at the receiver clock pulse rate. At the same time, it feeds the counter value representing the number of successful comparisons into a control unit 76 by means of a
5 line 74.

Control unit 76 receives from memory 61 the identity of the sampling instant which produced the first of the successful comparisons and it can therefore determine the time instant which is midway between the sampling instants corresponding to the first and last successful comparisons recorded by the counter 62. By means of a line 78, the control unit 76 rephases the clock
10 44 so that the first data sample taken by the sampling gate 42 at the lower sampling rate (that is, at the clock pulse rate) occurs at the next following time instant corresponding to this midway time instant (that is, in the next bit period).

This process bit-synchronises the receiver clock pulse waveform with the incoming data as will be described in more detail now with reference to Fig. 4.
15 On the assumption that the value of x and the form of the preamble $P_a$ of waveform 4B are both such that it is not possible for comparator 48 to record a successful comparison until it has compared all the y (or 6 in this example) bits of the incoming preamble with the stored preamble, it is apparent that the comparator 48 will not be able to start recording successful comparisons until time $t_3$ (that is, at the start of the last bit of the incoming preamble). At and
20 after $t_3$, the comparator 48 is able to compare six bits of received preamble with the stored preamble and is therefore comparing enough bits to be able to determine whether at least x of them agree with the bits of the stored preamble.

Table A below shows the values of the data samples corresponding respectively to waveforms $4F_1$ to $4F_8$ which will be passed to the comparator 48 at the time instants $t_3$ to $t_{11}$.
25

TABLE A

| Waveform | Corresponding time | Corresponding register | Data samples fed to comparator from register |
|---|---|---|---|
| $4F_3$ | $t_3$ | 28 | 000001 |
| $4F_4$ | $t_4$ | 30 | 001011 |
| $4F_5$ | $t_5$ | 32 | 001011 |
| $4F_6$ | $t_6$ | 34 | 001011 |
| $4F_7$ | $t_7$ | 36 | 001011 |
| $4F_8$ | $t_8$ | 38 | 001011 |
| $4F_1$ | $t_9$ | 24 | 001011 |
| $4F_2$ | $t_{10}$ | 26 | 001011 |
| $4F_3$ | $t_{11}$ | 28 | 000010 |

As explained, the comparator 48 compares each of these sequences of data samples with the pre-stored preamble in register 20 which is 0 0 1 0 1 1.
45 Table B below shows the output produced by the comparator 48 in response to the eight successive comparisons.

TABLE B

| Time instant | Comparator 48 output |
|---|---|
| $t_3$ | 0 |
| $t_4$ | 1 |
| $t_5$ | 1 |
| $t_6$ | 1 |
| $t_7$ | 1 |
| $t_8$ | 1 |
| $t_9$ | 1 |
| $t_{10}$ | 1 |
| $t_{11}$ | 0 |

From Table B, it is apparent that the counter 62 will have attained a count of 7 at time instant $t_{10}$. At time instant $t_{11}$ the comparator 48 will record an unsuccessful comparison, and the count
65 of counter 62 (that is, 7) will be read out and compared in comparator 68 with the threshold

value (six in this example). This comparison will be successful, and threshold unit 68 will
therefore activate control unit 76, and switch out the multiplier 46. The identity of the time
instant corresponding to the first successful comparison stored in the counter 62 will be time
instant $t_4$. Therefore, the time instant midway between $t_4$ and $t_{10}$ is $t_7$ (the seventh sampling
5  instant) and the control unit 76 will therefore re-phase the clock pulse 44 so that the next                5
sample taken at the lower rate by the sampling gate 42 will occur at time $T_1$ which is the time
when the seventh sampling instant occurs in the next bit period. Therefore, the first bit of the
message will be correctly sampled at its mid-point and the clock pulse source 44 of the receiver
has been correctly synchronised. Times $t_{13}$ and $t_{14}$ show the next times that the sampling gate
10  42 (sampling now at the bit rate) samples the incoming data.                                                10
     Fig. 3 illustrates how comparator 48A controls components corresponding to those controlled
by comparator 48 and these components have the same reference numerals but are distin-
guished by the suffix A. Their operation corresponds to that of the components controlled by
comparator 48 and will not be described.
15     Some of the system illustrated in block diagram form in Fig. 3 can be implemented by a              15
microprocessor operating under software control. For example, the recording of the number of
successful comparisons made by the comparators 48 and 48A, and the computation carried out
by the comparators 68 and 68A, and the control unit 76, of the correct time instant at which
the sampling gate 42 is to commence sampling at the lower rate, may be performed by the
20  microprocessor under software control.                                                                     20
     If the threshold number to which the comparators 68 and 68A respond, and which
determines the number of successful comparisons which must occur before bit-synchronisation
takes place, is made too high (too close to the number of samples, 8 in this case, taken per bit
period), then distortion of the incoming waveform may prevent its being recognised by either
25  comparator.                                                                                                25
     Fig. 5 shows how the registers 24 to 38 of Fig. 3 may be implemented by a 512 bit random
access memory for the case where y is 64 and the fast sampling rate is eight times the bit rate.
     The RAM is organised into eight 64-bit registers and the RAM has a 512-bit address counter
80 which is divided into a section 80A comprising the three least significant bits of the address
30  of each register stage and a section 80B comprising the six most significant bits of the address        30
of each register stage.
     As each data sample is received by the distribution unit 40, the latter feeds the data sample
into the appropriate one of the eight 64-bit registers into which the RAM is organised and
increments the address counter 80 by 1. Immediately thereafter, and before the next data
35  sample is received, the six most significant counter stages 80B are rapidly counted through a          35
complete cycle by the timing pulses on line 60, that is, stepped on by 64 pulses. During this
process, the three least significant counter stages 80A are held static. As the counter stages
80B are incremented in this way, they successively address the 64 stages of the appropriate one
of the registers in the RAM and the bit samples are fed out to the comparators 48 and 48A
40  (Fig. 3) on the channel 50.                                                                                40
     When the next data sample is received, the distribution unit 40 directs it into the next 64-bit
register in the RAM and increments the counter, and the process repeats.
     In this way, the three least significant stages of the counter 80 identify the particular one of
the eight registers which is active during each sampling time instant while the six most
45  significant stages 80B are used to address each of the stages of that register in turn to output its  45
stored data samples to the comparators 48 and 48A.
     In order to generate the preambles $P_a$ and $P_b$ stored in registers 20 and 22 (Fig. 3), the two
basic sequences I and II (from which all the preambles are generated as explained earlier) may
be stored in each receiver. Each receiver can then be programmed or otherwise instructed to
50  generate the two preambles to be stored in its registers 20 and 22 by instructing it to add the       50
two basic sequences I and II together, after phase-shifting one of them with respect to the other
by a predetermined number of bit periods.
     From the foregoing, it will be apparent how the preample of each data message transmitted
by the transmitter 5 is used simultaneously to perform the three functions specified above, that
55  is, (a) character framing (identifying the beginning of the data message), (b) addressing either a     55
specific one or all of the receivers and (c) bit-synchronising the addressed receiver or receivers.

CLAIMS
     1.   A data transmission system for transmitting data messages from a data transmitter to a
60  specific one of a plurality of receivers to which the transmitter is connected by a transmission        60
link, comprising preamble generating means in the transmitter for immediately preceding each
data message with a predetermined preamble which is intended to be recognisable by one of
the receivers, to which the message is directed, but not by others of the receivers to which the
message is not directed, recognition means in each of the receivers for testing for recognition
65  each preamble received via the transmission link, and synchronisation means in each receiver          65

which is responsive to each recognised preamble for synchronising that receiver with the data message immediately following the preamble.

2. A system according to claim 1, in which the recognition means is arranged to recognise a preamble if it recognises at least a predetermined part thereof, the said part being such in
5 relation to expected errors in the transmission link, that the probability is high that the   5
recognition means will recognise the correct preamble and being such that the probability is low that the recognition means will recognise noise as the correct preamble.

3. A system according to claim 2, in which the preamble generating means generates each preamble as a plurality of data bits, and each recognition means comprises means in each
10 receiver for comparing each preamble received on the transmission link with a predetermined   10
preamble stored in that receiver, and means for indicating recognition when at least a predetermined plurality of bits forming the said predetermined part of the received preamble agree as to value and position with corresponding bits forming part of the stored preamble.

4. A system according to any preceding claim, in which the preamble generating means in
15 the transmitter includes means for generating a preamble which is intended to be recognisable   15
by a plurality of the receivers.

5. A data transmission system, comprising a data transmitter connected by a transmission link to a plurality of data receivers for sending data messages to any specific one of the receivers, preamble generating means at the transmitter for preceding each data message with a
20 selected one of a plurality of different predetermined preambles and for transmitting the selected   20
preamble to all the receivers immediately beore the data message, one of the preambles being recognisable by all the receivers and each of the remaining preambles being recognisable only by a specific one of the receivers, and recognition means in each receiver for recognising either the said one preamble or the respective one of the remaining preambles and, in response to
25 such recognition, for receiving the immediately following data message.   25

6. A system according to claim 5, in which the preamble generating means generates each preamble such that the Hamming distance between any pair of them is large.

7. A system according to claim 6, in which each preamble comprises a plurality of serial digits, and in which the preamble generating means comprises means responsive to two basic
30 sequences of serially arranged digits for carrying out a succession of adding operations each   30
comprising the addition of each of the digits of one of the basic sequences to a respective one of the digits of the other basic sequence, whereby each adding operation produces a respective one of the said preambles, the first adding operation comprising the addition of each digit in one basic sequence to the same serially numbered digit in the other basic sequence, the next
35 adding operation involving the addition of each digit in one of the basic sequences to the digit   35
in the other basic sequence having a serial number greater by one (with the last digit of the first sequence being added to the first digit of the second sequence), the third adding operation involving the addition of each digit in the first sequence to the digit of the second sequence having a serial number greater by 2 (with the penultimate and last digits of the first sequence
40 being added to the first and second digits, respectively, of the second sequence), and so on for   40
the remaining adding operations.

8. A system according to any one of claims 5 to 7, in which the recognition means in each receiver comprises means operative to compare the digits of an incoming transmitted preamble with the digits of the predetermined preamble of that receiver, and means for indicating
45 recognition when at least a predetermined block of incoming digits agrees digit by digit with a   45
corresponding block of the digits of the predetermined preamble, the predetermined block being such in relation to digits of the whole predetermined preamble and to the expected occurrence of transmission errors on the transmission link that the probability of any of the recognition means recognising the correct preamble is high and the probability of its recognising noise on
50 the transmission link as the correct preamble is low.   50

9. A data transmission system, comprising a data transmitter connected to a data receiver by a data transmission link, means in the transmitter for transmitting to the receiver a predetermined waveform having a predetermined frequency, means in the receiver and operative at a predetermined multiple of a reference frequency which is equal to the predetermined frequency
55 but not necessarily in phase therewith to produce successive amplitude samples of each cycle of   55
the predetermined waveform, means responsive to the samples to produce a plurality of pulse trains the first of which comprises pulses respectively dependent on the first amplitude sample in each period of the predetermined waveform, the second of which comprises pulses respectively dependent on the second amplitude sample of each cycle of the predetermined
60 waveforms, and so on for the remaining pulse trains, means operative to compare each pulse   60
train with a waveform corresponding to the predetermined waveform to determine which of the pulse trains have waveforms corresponding with the predetermined waveform and which do not, means operative in response to the pulse trains detected as having waveforms agreeing with the predetermined waveform to assess the serial position within a period of the reference frequency
65 of the samples producing those pulse trains to identify the central one of those serial positions.   65

and phase-shift means operative to phase-shift the reference frequency of the receiver to bring it into phase with the central one of those serial positions, whereby to synchronise the reference frequency of the receiver with the predetermined frequency.

10.    A system according to claim 9, including means for counting the number of pulse trains
5 which are detected as having waveforms agreeing with the predetermined waveform and for        5
preventing operation of the phase-shift means until the number counted is at least equal to a predetermined number which is less than the number of the samples within each period of the reference frequency.

11.    A data transmission system substantially as described with reference to Figs. 1 and 2 of
10 the accompanying drawings.
12.    A data transmission system substantially as described with reference to all the Figures of       10
the accompanying drawings.